

It is claimed:

1        1.    In a tunable receiver, the improvement comprising:  
 2        a filter circuit having a frequency response determined by  
 3        a value of at least one passive circuit element of a  
 4        predetermined type in the filter circuit;  
 5        a plurality of circuit elements of the predetermined type;  
 6        a plurality of switches, each associated with a respective  
 7        circuit element for switching the respective circuit element  
 8        into the filter circuit to vary the frequency response of the  
 9        filter circuit;  
 10       a digital interface responsive to digital input signals to  
 11       control the plurality of switches;  
 12       the plurality of circuit elements of the predetermined  
 13       type, the plurality of switches and the digital interface being  
 14       incorporated in a single integrated circuit.

1       2.    The digitally tunable filter of claim 1 wherein the  
 2       digital interface may couple any of the plurality of circuit  
 3       elements individually, in parallel, or in series with each  
 4       other into the filter circuit.

1       3.    The digitally tunable filter of claim 2 wherein the  
 2       values of the plurality of circuit elements are in a binary  
 3       progression.

1       4.    The digitally tunable filter of claim 3 wherein the  
 2       circuit elements are capacitances.

1       5.    The digitally tunable filter of claim 1 wherein the  
 2       digital interface includes conversion circuitry responsive to

3 the digital input signals to convert the digital input signals  
4 to switch control signals.

1 6. The digitally tunable filter of claim 1 wherein the  
2 digital interface includes conversion circuitry responsive to  
3 the digital input signals to convert the digital input signals  
4 to switch control signals in accordance with a predetermined  
5 calibration of the digitally tunable filter.

1 7. The digitally tunable filter of claim 1 wherein the  
2 filter circuit is comprised of at least one resonator.

1 8. The digitally tunable filter of claim 7 wherein the  
2 resonator is comprised of an inductor - capacitance network.

1 9. The digitally tunable filter of claim 8 wherein the  
2 circuit elements are capacitances.

1 10. The digitally tunable filter of claim 9 wherein the  
2 values of the plurality of circuit elements are in a binary  
3 progression.

1 11. The digitally tunable filter of claim 8 wherein the  
2 digitally tunable filter circuit, including one or more  
3 inductors, is incorporated in the single integrated circuit.

1 12. The digitally tunable filter of claim 8 wherein one  
2 or more of the inductors are printed inductors on a printed  
3 circuit board.

1 13. The digitally tunable filter of claim 12 wherein the  
2 printed circuit board is a land grid array (LGA).

1        14. The digitally tunable filter of claim 8 wherein one  
 2 or more of the inductors are surface mount inductors, and  
 3 wherein the rest of the digitally tunable filter circuit is  
 4 incorporated in the single integrated circuit.

1        15. The digitally tunable filter of claim 8 wherein one  
 2 or more of the inductors are printed inductors on a printed  
 3 circuit board and one or more of the inductors are surface  
 4 mount inductors attached to said printed circuit board, and the  
 5 rest of the digitally tunable filter circuits are incorporated  
 6 in the single integrated circuit.

1        16. The digitally tunable filter of claim 15 wherein the  
 2 printed circuit board is a land grid array (LGA).

1        17. A digitally tunable filter comprising:  
 2        a filter circuit having an inductance - capacitance  
 3 network with a frequency response determined by a value of at  
 4 least one capacitive element in the filter circuit;  
 5        a plurality of capacitive elements;  
 6        a plurality of switches, each associated with a respective  
 7 capacitive element for switching the respective capacitive  
 8 element into the filter circuit to vary the frequency response  
 9 of the filter circuit;  
 10       a digital interface responsive to digital input signals to  
 11 control the plurality of switches;  
 12       the filter circuit, the plurality of capacitive elements  
 13 of the predetermined type, the plurality of switches and the  
 14 digital interface being incorporated in a single integrated  
 15 circuit.

1        18. The digitally tunable filter of claim 17 wherein the  
2 digital interface may couple any of the plurality of capacitive  
3 elements individually, in parallel, or in series with each  
4 other into the filter circuit.

1        19. The digitally tunable filter of claim 18 wherein the  
2 values of the plurality of capacitive elements are in a binary  
3 progression.

1        20. The digitally tunable filter of claim 17 wherein the  
2 digital interface includes conversion circuitry responsive to  
3 the digital input signals to convert the digital input signals  
4 to switch control signals.

1        21. The digitally tunable filter of claim 17 wherein the  
2 digital interface includes conversion circuitry responsive to  
3 the digital input signals to convert the digital input signals  
4 to switch control signals in accordance with a predetermined  
5 calibration of the digitally tunable filter.

1        22. The digitally tunable filter of claim 17 wherein the  
2 inductance comprises one or more printed inductors on a printed  
3 circuit board.

1        23. The digitally tunable filter of claim 17 wherein the  
2 inductance comprises one or more printed inductors on a printed  
3 circuit board and one or more surface mount inductors attached  
4 to said printed circuit board.

1        24. The digitally tunable filter of claim 23 wherein the  
2 printed circuit board is a land grid array (LGA).

1        25. A method of calibrating a digitally tunable filter  
2 used in a receiver, the method comprising:  
3        adjusting a plurality of digital control codes associated  
4 with said digitally tunable filter;  
5        measuring frequency responses of said digitally tunable  
6 filter for the various digital control codes;  
7        characterizing the frequency response of said digitally  
8 tunable filter by means of a second set of digital codes; and  
9        storing said second set of codes in a memory.

1        26. The method of calibrating a digitally tunable filter  
2 of claim 25, wherein said frequency responses are comprised of  
3 pass bands which pass frequencies associated with desired  
4 signals and rejection bands which attenuate frequencies  
5 associated with undesired signals.

1        27. The method of calibrating a digitally tunable filter  
2 of claim 26, wherein said rejection bands attenuate frequencies  
3 associated with the image signals of said desired signals.

1        28. The method of calibrating a digitally tunable filter  
2 of claim 26, wherein said digitally tunable filter comprises  
3 one or more digitally tunable filter resonators.

1        29. The method of calibrating a digitally tunable filter  
2 of claim 28, wherein said digitally tunable filter resonators  
3 comprise one or more digitally tunable filter LC networks.

1        30. The method of calibrating a digitally tunable filter  
2 of claim 29, wherein said digitally tunable filter LC networks  
3 are implemented on a monolithic integrated circuit.

1        31. The method of calibrating a digitally tunable filter  
2 of claim 29, wherein said digitally tunable filter LC networks  
3 comprise networks of fixed value inductors and digitally  
4 controlled capacitors.

1        32. The method of calibrating a digitally tunable filter  
2 of claim 31, wherein said networks of fixed value inductors and  
3 digitally controlled capacitors are implemented on a monolithic  
4 integrated circuit.

1        33. The method of calibrating a digitally tunable filter  
2 of claim 31, wherein said networks of fixed value inductors and  
3 digitally controlled capacitors comprise digitally controlled  
4 capacitors implemented on a monolithic integrated circuit and  
5 inductors external to said monolithic integrated circuit.

1        34. The method of calibrating a digitally tunable filter  
2 of claim 25, wherein said second set of codes are stored in a  
3 memory on an integrated circuit wherein said digitally tunable  
4 filter is located.

1        35. The method of claim 34 wherein each of the second set  
2 of codes are accessed by a respective one of the various  
3 digital control codes.

1        36. For use in a digitally tunable circuit, the  
2 improvement comprising:  
3        an integrated circuit having:  
4        a plurality of capacitor banks, each capacitor bank having  
5 a plurality of capacitors having capacitances in a binary  
6 progression;

7       a plurality of switches coupled to each capacitor bank,  
8       each plurality of switches being controllable to switch one or  
9       more than one of the capacitors in the respective capacitor  
10      bank in parallel into another circuit; and,  
11      a control circuit coupled to receive control information  
12      and to control the plurality of switches in response thereto.

1       37. The improvement of claim 36 wherein the switches are  
2      FET switches.

1       38. The improvement of claim 36 wherein the control  
2      comprises a shift register coupled to serially receive and  
3      store a switch control word, and to control each switch by a  
4      respective bit of the control word.

1       39. The improvement of claim 36 wherein the control  
2      comprises a controller and memory.

1       40. The improvement of claim 39 wherein the controller is  
2      coupled to receive a switch control word and to control each  
3      switch responsive to the switch control word, the memory being  
4      coupled to the controller to store a switch control word  
5      received by the controller.

1       41. The improvement of claim 40 wherein the control is  
2      coupled to a serially receive a switch control word.

1       42. The improvement of claim 39 wherein the controller is  
2      coupled to receive calibration information and to store the  
3      calibration information in the memory, the controller also  
4      being coupled to receive any of a plurality of predetermined  
5      control words, each associated with a respective set of

6 capacitance values to be switched into another circuit, and to  
7 use the calibration information stored in memory to control the  
8 switches to obtain the capacitance values associated with each  
9 predetermined control word received.

1       43. The improvement of claim 42 wherein the control is  
2 coupled to a serially receive a switch control word.